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ENERGY CONV DEVICES INC *EP -161-555-A
14.05.84-US-609640 (+US-637435) *(21.10.85)* H01I-21/84 H01I-27/8 H01I-29/4
Thin film semi-amorphous FET - for video frequency, LCD, and memory applications
C85-125933 E(AT BE CH DE FR GB IT)

Thin film FET, capable of video switching rates, is described. The body of the FET consists of a semi-amorphous semiconductor, which may be either Si or Si/Ge alloy. The body of the semiconductor is deposited on the insulating substrate by molecular beam epitaxy at 450-500°C. It is annealed at 500°C in an atmos. of either F_2 or H_2, which may also include N_2.

USE

The transistor has high field effect mobility, and may be made using 10μ lithography, permitting large area application at 50 MHz switching rates. The high speed enables it to be used in LCDs and fast read out memories.

EMBODIMENTS

The transistor includes a body of semiconductor material (54) which is either Si or Si/Ge alloy; the material is semi-amorphous, the degree of order being between that of the amorphous and single crystal phases. The body is formed by molecular beam epitaxy deposition at 450-500°C and at a pressure not greater than 10^{-8} torr, resulting in a grain size of 2000-3000 Å. It is then annealed at 500°C and 0.1-0.5 Torr in an H_2 atmosphere, which may include N_2 or in an F_2 or H_2 plasma.

The source (56) and the drain (58) are deposited on the body (54) and consist of an amorphous Si alloy doped n type with phosphorus and containing H_2 and/or F_2. They may also be formed by depositing metal on the body so as to form a Schottky barrier junction.

The gate insulator (60) is formed on the source, drain and body. It may either be Si_3N_4 or SiO_x and is deposited by glow discharge from a mixture of N (for Si_3N_4) or O (for SiO_x) and SiH_4. The gate electrode (62) is formed on the gate insulator.

A means of selectively addressing a 2D matrix array is also described. (21pp 1716DwgNo1/2).

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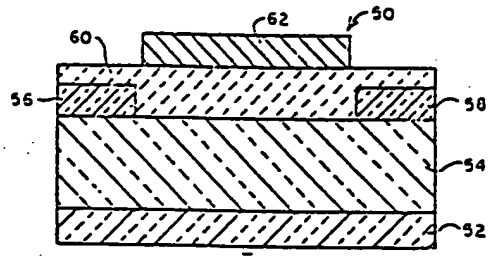

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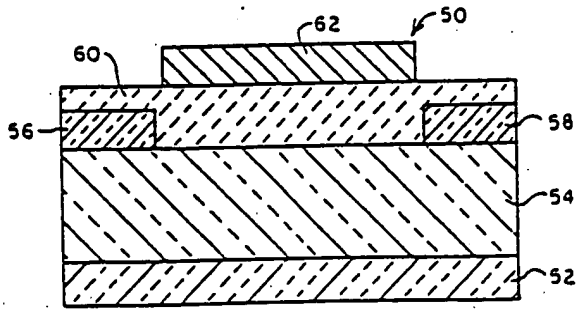
(54) Thin film field effect transistor and method of making same.

(57) There is disclosed a film field effect transistor which can be operated at fast switching rates for use, for example, in video display applications. The transistor includes a body of silicon semiconductor material having a structure more ordered than amorphous material and less ordered than single crystalline material. The source and drain of the transistor comprise rectifying contacts formed on the body of silicon semiconductor material. Also disclosed are a method of making the transistor and an electronically addressable array system utilizing the transistor to advantage.



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THIN FILM FIELD EFFECT TRANSISTOR AND METHOD OF MAKING SAME

FIELD OF THE INVENTION

The present invention generally relates to thin film field effect transistors and a method of making the transistors. The invention more particularly relates to thin film field effect transistors which are capable of operating at high switching speeds for applications where high speed operation is essential. Such applications include matrix array addressing systems wherein the addressing circuits are required to operate at video rates.

BACKGROUND

Electronic matrix arrays find considerable application in systems such as, for example, liquid crystal displays and high density memories. Such systems generally include X and Y address lines which are vertically spaced apart and cross at an angle to form a plurality of crossover points. Associated with each crossover point is an element to be selectively addressed. The elements can be, for example, the liquid crystal display pixels of a liquid crystal

display or the memory cells of an electronically addressable memory array.

Some form of isolation device is generally associated with each array element. The isolation elements permit the individual elements to be selectively addressed by the application of suitable read potentials between respective pairs of the X and Y address lines.

Amorphous semiconductor thin film field effect transistors have found wide usage for the isolation devices in such arrays. Thin film field effect transistors formed from deposited semiconductors, such as amorphous silicon alloys are ideally suited for such applications because they exhibit a very high dark resistivity and therefore have very low reverse leakage currents. The reverse leakage currents are so low that very high on to off current ratios are made possible for effectively isolating the non-addressed array elements from the array elements being addressed.

While prior art thin film field effect transistors formed from amorphous semiconductor alloys are ideally suited as isolation devices in addressable arrays, they are not so ideally suited for use in forming the addressing circuitry required for the selective addressing of the array elements. One reason for this is that these devices have not exhibited the switching speeds required for these applications.

For many applications, the components forming the addressing circuitry of electronically addressable arrays are required to switch at video rates, on the order of 50 megahertz, for example. Such is the case particularly in liquid crystal displays or fast read-out memories. Structurally, thin film field effect transistors generally include source and drain

electrodes, a semiconductor material between the source and drain electrodes, and a gate electrode in proximity to the semiconductor but electrically insulated there from by a gate insulator. Current flow through the transistor between the source and drain is controlled by the application of a voltage to the gate electrode. The voltage on the gate electrode produces an electric field which accumulates a charged region near the semiconductor-gate insulator interface. This charged region forms a current conducting channel in the semiconductor through which the device current is conducted.

In thin film field effect transistors, both output current and operating speed are directly related to the structural configurations of the devices and to the field effect mobility of the semiconductor material. The output current is directly proportional to the field effect mobility and is almost always inversely proportional to the current conduction channel length. The maximum operating frequency of such a device is related to the channel length which is fixed by the spacing between the source and drain electrodes in a more complicated manner. The reason for this is that the operating frequency is not only related to the channel length, but is also dependent upon the total capacitance of the device. The total capacitance has basically two components, a fixed capacitance due to electrode overlap, and a dynamic capacitance that results when the current conduction channel is formed. The fixed capacitance is a direct function of the electrode overlap. The dynamic capacitance however is inversely proportional to the channel length. Since both the output current and the dynamic capacitance are both inversely proportional to the channel length, the maximum operating frequency should be inversely

proportional to the square of the channel length if the fixed capacitance is disregarded. But the fixed capacitance cannot be disregarded, and it remains an important frequency limiting factor. Fortunately, however, transistor configurations have been designed which minimize fixed capacitance. Field effect mobility, on the other hand, is generally fixed by the type of semiconductor used to form the device, and unfortunately, amorphous semiconductor alloys exhibit relatively low field effect mobilities on the order of .1 to 1. Hence, even though improved configurations have decreased the capicitance of amorphous semiconductor thin film transistors, the field effect mobilities of such devices essentially preclude their use in applications such as in addressing circuitry, where video rate switching is often required.

In summary, while amorphous semiconductor alloy thin film field effect transistors are ideally suited for many applications, such as for isolating matrix array elements to be selectively addressed, they are not suited for use in applications where video rate switching is required in association with other components which would be adversely affected by the processing of the devices. For this particular and important application, a new and improved thin film field effect transistor is required. The improved transistor must include a semiconductor material having high field effect mobility. It preferably should be adapted to be fabricated using commercially acceptable processes and conventional 1.0 micron photolithography permitting large area application while still exhibiting fast switching rates at, for example, video rates of about 50 Mhz.

Thin film transistors have been made with polycrystalline silicone and reported in the literature. See for example, "Thin-film transistors

on molecular-beam-deposited polycrystalline silicon", Matsui et. al., 55 J. Applied Physics 1590, March 15, 1984. Matsui disclosed a thin film transistor with source and drain regions formed in polycrystalline silicon by ion implantation which is generally not a commercially acceptable process.

SUMMARY OF THE INVENTION

The invention provides a thin film field effect transistor capable of operating at video switching rates. The transistor comprises a body of semiconductor material including silicon. The semiconductor material has a structure more ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material. The transistor further includes source and drain elements forming rectifying contacts with the body of semiconductor material and a gate electrode adjacent to and insulated from the body of semiconductor material.

The source and drain are formed on the body of silicon semiconductor material. The source and drain elements can oe deposits of a doped semiconductor on the body of semiconductor material.

The doped deposits for the source and drain are preferably n-type when the body of semiconductor material is slightly p-type and p-type when the body semiconductor material is slightly n-type.

Alternately, source and drain electrodes can be formed as deposits of metal on the body of semiconductor material.

The body of semiconductor material can further include compensating elements such as hydrogen or fluorine. The body of semiconductor material can also be an alloy of silicon and germanium.

The invention further provides a system for selectively addressing each element of an array of elements. The system includes a first set of address lines, and a second set of address lines spaced from and crossing at an angle to the first set of address lines to form a plurality of crossover points therewith wherein each crossover point is associated with a given one of the elements to be addressed. The system further includes addressing circuitry coupled to the first and second sets of address lines for selectively applying addressing potentials to respective pairs of the first and second sets of address lines. The addressing circuitry includes at least one thin film field effect transistor comprising a body of semiconductor material including silicon or an alloy of silicon and germanium, for example. The semiconductor material has a structure more ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material.

The invention further provides a method of making a thin film field effect transistor. The method includes the steps of forming a body of semiconductor material including silicon wherein the silicon semiconductor material is formed with a structure more ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material, forming source and drain elements in rectifying contact with the body of semiconductor material, and forming a gate electrode adjacent to and insulated from the body of semiconductor material.

The method can also include the step of forming a body of semiconductor alloy material including a combination of silicon and germanium.

The body of semiconductor material is preferably formed by depositing the semiconductor

material onto a substrate which is heated to a temperature between 450°and 500°C. The body of semiconductor material is preferably deposited by molecular beam epitaxy.

The semiconductor body can be annealed prior to forming the drain and source elements in a hydrogen gas atmosphere, in an atmosphere of hydrogen gas and a forming gas, in a hydrogen plasma, or in a fluorine plasma. The semiconductor body can be annealed at a temperature of about 500°C and at a pressure between .1 and .5 Torr.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross-sectional side view of a thin film field effect transistor embodying the present invention; and

Fig. 2 is a schematic diagram, partially in block form, of an electronically addressable matrix array of the type which can utilize the thin film field effect transistor of the present invention to advantage.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A thin film field effect transistor 50 structured in accordance with the present invention is illustrated in Fig. 1. The transistor 50 includes a substrate 52 which can be formed from an insulating material, such as glass, for example. Formed on the substrate 52 is a body 54 of semiconductor material. The body 54 of semiconductor material includes at least silicon or an alloy of silicon and other elements such as germanium. The body of semiconductor material 54 is formed with a structure which is more

ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material. Such material can include, for example, microcrystalline or polycrystalline semiconductor material. By the term "amorphous" is meant an alloy or material which has long-range disorder, although it may have short or intermediate order or even contain at times some crystalline inclusions.

The body of semiconductor material 54 can be formed to have such structure by depositing the silicon or silicon and germanium semiconductor material by an MBE (molecular beam epitaxy) deposition of the type well known in the art. The deposition is preferably achieved using a target of powdered polycrystalline silicon or silicon and germanium. The substrate 52 is preferably heated to a temperature between 450°C and 500°C and the deposition pressure is preferably maintained at 10^{-8} Torr or less. Under these deposition conditions, the deposited body of semiconductor material 54 will have indeed a more ordered structure than amorphous material and a less ordered structure than single crystalline material. More specifically, the silicon or silicon and germanium alloy semiconductor material thus deposited will have a grain size ranging from 2,000 angstrom to 3,000 angstrom.

When the target of powdered polycrystalline silicon or silicon and germanium is intrinsic or not intentionally doped, the resulting body of deposited silicon or silicon and germanium material is slightly p-type (-type). If the target of polycrystalline silicon or silicon and germanium has been doped to be lightly n-type, the resulting body of deposited silicon or silicon and germanium material is slightly n-type.

After the body of semiconductor material 54

is formed, it can be postcompensated by annealing in an atmosphere of hydrogen, an atmosphere of hydrogen and a forming gas such as nitrogen, in a hydrogen plasma, or in a fluorine plasma. The annealing process is preferably accomplished at a temperature of about 500 C and a pressure between .1 to .5 Torr.

By annealing the body 54 of semiconductor material as described above, the compensating elements such as hydrogen or fluorine are diffused into the body 54 of semiconductor material to compensate for dangling bonds or other structural defects which may exist in the material. The material after annealing can thus be considered a silicon or a silicon and germanium semiconductor alloy incorporating either hydrogen or fluorine. The annealing in a hydrogen and nitrogen atmosphere is preferred inasmuch as the nitrogen serves as a forming gas to reduce defects at the grain boundaries of the material.

The transistor 50 further includes a source 56 and a drain 58. In accordance with this preferred embodiment of the present invention, the source and drain 56 and 58, respectively, take the form of deposits of doped semiconductor material. Preferably, the doped semiconductor material comprises an amorphous silicon alloy containing hydrogen and/or fluorine. The doped semiconductor forming the source and drain 56 and 58 is preferably doped n-type with phosphorus. This amorphous semiconductor alloy is preferably deposited in a manner as fully described in the aforementioned U.S. Patent No. 4,226,898. Preferably, the doped semiconductor material forming the source and drain 56 and 58 includes fluorine. Such material has been found to be a superior -type material in that it has very high electrial conductivity and exhibits substitutional doping characteristics. With the body 54 of semiconductor

material being p-type and the source 56 and drain 58 being formed from n-type amorphous silicon alloy material, the source and drain 56 and 58 will form rectifying contacts with the body 54 of semiconductor material to the end of reducing the reverse leakage of the device.

If the body of the semiconductor material is slightly n-type, the source 56 and drain 58 can be formed of p-type amorphous silicon alloy material so as to form the rectifying contacts. In this case boron is used as the dopant.

The use of a source and a drain formed of amorphous silicon alloys as disclosed above deposited onto a body such as 54 results in a number of advantages. Depositing an amorphous semiconductor alloy onto the body 54 to form the source 56 and the drain 58 is faster than processes where the source and drain are implanted into the body. Further, deposition of amorphous alloys to form source and drain regions can readily be carried out with respect to many transistors to be formed over a wide area. The amorphous silicon can also be tailored to have differing characteristics for various applications.

Formed over the source 56, drain 58, and the body 54 of silicon or silicon and germanium semiconductor alloy material is a gate insulator 60. The gate insulator 60 can be formed from silicon oxide or silicon nitride. The gate insulator 60 can be deposited by a glow discharge process as disclosed, for example, in U.S. Patent No. 4,226,898 which issued on October 7, 1980 in the names of Stanford R. Ovshinsky and Arun Madan for Amorphous Semiconductors Equivalent To Crystalline Semiconductors. When the gate insulator 60 is formed from a silicon oxide, it can be deposited by the glow discharge decomposition of, for example, silane (SiH_4) and oxygen. When the

gate insulator is formed from silicon nitride, it can be deposited from the glow discharge decomposition of silane and ammonia (NH_3).

The device 50 is completed with the formation of a gate electrode 62 over the gate insulator 60. The gate electrode 62 can be formed from any conductive metal such as aluminum or chromium.

As an alternate to the use of an amorphous silicon alloy film to form the source 56 and drain 58, when the body 54 is n-type, the source and drain can be formed of deposits of a high work function metal such as platinum or palladium. If the source 56 and drain 58 are formed of a high work function metal they will form rectifying contacts with the body 54 of silicon semiconductor material and serve the same function as do the rectifying contacts formed when the amorphous semiconductor alloy film is used to form the source and drain regions. When the body 54 is p-type, the source 56 and drain 58 can be formed of low work function metals such as magnesium or ytterbium. These metals can be deposited by evaporation.

With respect the embodiment of Fig. 1, the body 54 of semiconductor material is preferably deposited to a thickness of 2000 angstrom to 1 micron. The source 56 and drain 58 are preferably formed to have thicknesses on the order of 100 to 500 angstrom when formed from a p-type or an n-type region or 100 to 1000 angstrom when formed from a high or low work function metal. The gate insulator 60 is preferably formed to have a thickness ranging between 300 to 5000 angstrom for disposing the gate electrode 62 adjacent the body 54 of semiconductor material and electrically insulated therefrom.

When it is desired to cause the thin film field effect transistor 50 to conduct, assuming it has a slightly p-type body 54, a positive potential is

applied to both the gate 62 and the source 56 of the device. The positive gate potential will cause a carrier inversion to take place within the body 54 of the semiconductor material so that electron accumulation takes place at the interface between the gate insulator 60 and the body 54 of semiconductor material. This charge accumulation forms the current conducting channel within the device for conducting the device current between the source 56 and drain 58.

When it is desired to terminate conduction within the device, the positive gate potential is removed to cause the accumulated charge at the interface of the gate oxide 60 and the body 54 of semiconductor material to be depleted. When this occurs, the current will cease flowing between the source 56 and drain 58. Because the source and drain form rectifying contacts with the body 54 of semiconductor material, they will preclude carrier injection in the reverse direction to thereby minimize the reverse leakage current of the device 50.

Fig. 2, illustrates a system 70 which can utilize the thin film field effect transistor 50 of the present invention to advantage. The system 70 is of the type which includes a plurality of X address lines 72, 74, 76, 78, 80, and 82 and a plurality of Y address lines 84, 86, 88, 90, and 92. The X and Y address lines are vertically spaced with respect to each other and cross at an angle to form a plurality of crossover points such as crossover point 94 formed by X address line 74 and Y address line 84.

Associated with each crossover point is an array element, such as element 96 associated with crossover point 94. Also associated with each crossover point is an isolation device such as a field effect transistor 98. As previously described, the isolation device, such as field effect transistor 98,

serves to permit selective addressing of the array elements, such as element 96. The isolation device 98 essentially isolates the non-addressed elements from the elements being addressed. Also as previously described, the thin film field effect transistor isolating devices preferably take the form of amorphous silicon alloy thin film field effect transistors because such transistors exhibit an extremely low reverse leakage. As illustrated in Fig. 2, the gate of transistor 98 is coupled to the X address line 74. The source of transistor 98 is coupled to Y address line 84. The drain of transistor 98 is coupled to the element 96 to be addressed and the opposite side of the element 96 is coupled to a common potential, such as ground potential.

Associated with each of the X address lines 72 through 82 is an X addressing circuit 102 and associated with each of the Y address lines 84 through 92 is a Y addressing circuit 104. Addressing circuits of this type can include the thin film field effect transistors of the present invention to distinct advantage. Circuits of this type utilizing field effect transistors are disclosed, for example, in an article entitled "A Liquid Crystal TV Display Panel With Drivers" which was published in SID Digest, Vol. 82, at pages 48 and 49. The X addressing circuit 102 and Y addressing circuit 104 provide read potentials between respective pairs of the X address lines and Y address lines so as to selectively address the elements of the array such as element 96. When the array is a liquid crystal display, the element 96 is a liquid crystal display pixel and when the array is a memory matrix, the element 96 can take the form of an individual memory cell.

From the foregoing, it can be appreciated that the present invention provides a thin film field

effect transistor which provides high-speed operation, as for example, switching speeds at video rates. Therefore, the thin film field effect transistor of the present invention is ideally suited for use in addressing circuitry for liquid crystal video displays or fast readout electronically addressable memory arrays. The thin film field effect transistor of the present invention can be formed by using conventional 10 micron photolithography. This renders the devices ideally suited for commercial and large area applications.

CLAIMS

1. A thin film field effect transistor (50) of the type having a body (54) of semiconductor material, a source (56) and a drain (58) forming rectifying contacts with said body of semiconductor material, and a gate electrode (52) adjacent to and insulated from said body of semiconductor material, said transistor (50) being characterized by said body of semiconductor material including at least silicon, said semiconductor material having a structure more ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material and by said source and drain being formed on said body of amorphous semiconductor material.

2. A thin film field effect transistor (50) as defined in Claim 1 further characterized by said body (54) of semiconductor material also including germanium.

3. A thin film field effect transistor (50) as defined in Claim 1 further characterized by said source (56) and drain (58) being deposited on said body (54) of semiconductor material.

4. A thin film field effect transistor (50) as defined in Claim 3 further characterized by said source (56) and drain (58) comprising deposits of a metal which forms rectifying Schottky barrier junctions with said body of semiconductor material.

5. A thin film field effect transistor (50) as defined in Claim 1 further characterized by said source (56) and drain (58) being formed as doped regions on said body (54) of semiconductor material and by said body being of a first conductivity type and said doped regions being of an opposite conductivity type.

6. A thin film field effect transistor (50) as defined in Claim 5 further characterized by said source (56) and drain (58) comprising deposits of a doped semiconductor on said body (54) of semiconductor material.

7. A thin film field effect transistor (50) as defined in Claim 6 further characterized by said doped semiconductor deposits (56,58) comprising an amorphous semiconductor alloy.

8. A thin film field effect transistor (50) as defined in Claim 7 further characterized by said amorphous semiconductor alloy (56,58) including silicon.

9. A thin film field effect transistor (50) as defined in Claim 8 further characterized by said amorphous silicon alloy (56,58) including hydrogen or fluorine.

10. A thin film field effect transistor (50) as defined in Claim 8 further characterized by said amorphous silicon alloy (56,58) including fluorine.

11. A thin film field effect transistor (50) as defined in Claim 1 further characterized by said body (54) of semiconductor material further including hydrogen.

12. A thin film field effect transistor (50) as defined in Claim 1 further characterized by said body (54) of semiconductor material further including fluorine.

13. A system (70) for selectively addressing each element (96) of an array of elements, said system being of the type having a first set of address lines (72,74,76,78,80,82), a second set of address lines (84,86,88,90,92) spaced from and crossing at an angle to said first set of address lines to form a plurality of crossover points (94)

therewith, each such crossover point being associated with a given one of said elements to be addressed, and addressing circuitry (102,104) coupled to said first and second sets of address lines for selectively applying addressing potentials to respective pairs of said first and second sets of address lines; said system being characterized by said addressing circuitry including at least one thin film field effect transistor (50) comprising a body (54) of semiconductor material, said body including at least silicon with said semiconductor material having a structure more ordered than amorphous semiconductor material and less ordered than single crystalline semiconductor material, a source (56) and a drain (58) formed as rectifying contacts on said body of semiconductor material, and a gate electrode (62) adjacent to and insulated from said body of semiconductor material.

14. A method of making a thin film field effect transistor (50), said method being of the type including forming a body (54) of semiconductor material, forming a source (56) and a drain (58) in rectifying contact with said body, and forming a gate electrode (62) adjacent to and insulated from said body of semiconductor material, said method being characterized by forming said body of semiconductor material from a material including at least silicon, said semiconductor material being formed with a structure more ordered than amorphous silicon semiconductor material and less ordered than single crystalline silicon semiconductor material, and by forming said source and drain on said body.

15. A method as defined in Claim 14 further characterized by the body (54) of semiconductor material being formed by depositing the silicon semiconductor material onto a substrate (52)

and the substrate (52) being held at temperatures between 450°C and 500°C during the deposition thereof.

16. A method as defined in Claim 15 further characterized by the body (54) of semiconductor material being deposited by molecular beam epitaxy.

17. A method as defined in Claim 14 further characterized by including the step of annealing the semiconductor body (54) prior to forming the drain (58) and source (56).

18. A method as defined in Claim 17 further characterized by the semiconductor body (54) being annealed in a hydrogen gas atmosphere.

19. A method as defined in Claim 18 further characterized by the semiconductor body (54) being annealed at a temperature of about 500°C.

20. A method as defined in Claim 17 further characterized by the semiconductor body (54) being annealed in an atmosphere of a hydrogen gas and a forming gas.

21. A method as defined in Claim 20 further characterized by the forming gas being nitrogen.

22. A method as defined in Claim 20 further characterized by the semiconductor body (54) being annealed at a temperature of about 500°C.

23. A method as defined in Claim 17 further characterized by the semiconductor body (54) being annealed in a hydrogen plasma.

24. A method as defined in Claim 17 further characterized by the semiconductor body (54) being annealed in a fluorine plamsa.

25. A method as defined in Claim 14 further characterized by the source (56) and drain (58) being formed by depositing a doped semiconductor

in at least two spaced apart regions on the body (54) of semiconductor material.

26. A method as defined in Claim 25 further characterized by the doped semiconductor (56,58) comprising an amorphous semiconductor alloy.

27. A method as defined in Claim 26 further characterized by the amorphous semiconductor alloy (56,58) including silicon.

28. A method as defined in Claim 27 further characterized by the amorphous silicon alloy (56,58) including hydrogen.

29. A method as defined in Claim 27 further characterized by the amorphous silicon alloy (56,58) including fluorine.

30. A method as defined in Claim 14 further characterized by the source (56) and the drain (58) being formed by depositing a metal on at least two spaced apart regions on the body (54) of semiconductor material and by said metal being of a type which forms a rectifying Schottky barrier junction with said body of semiconductor material.

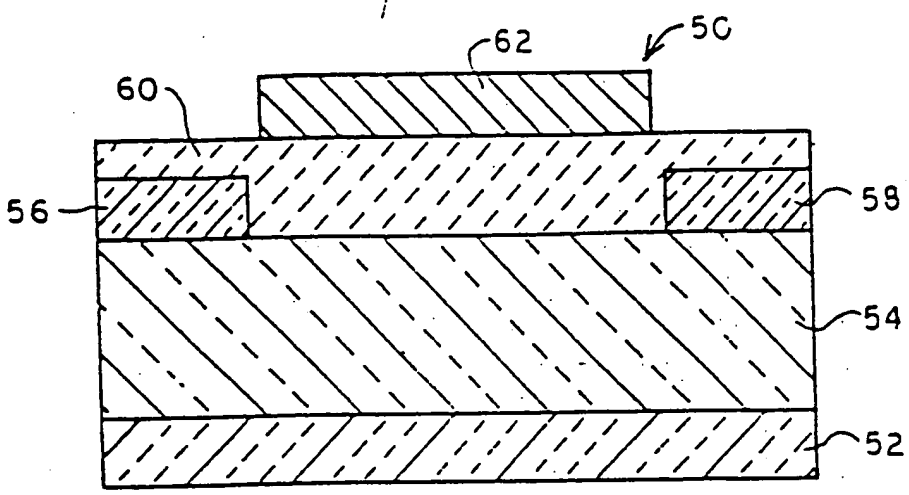
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FIG. 1

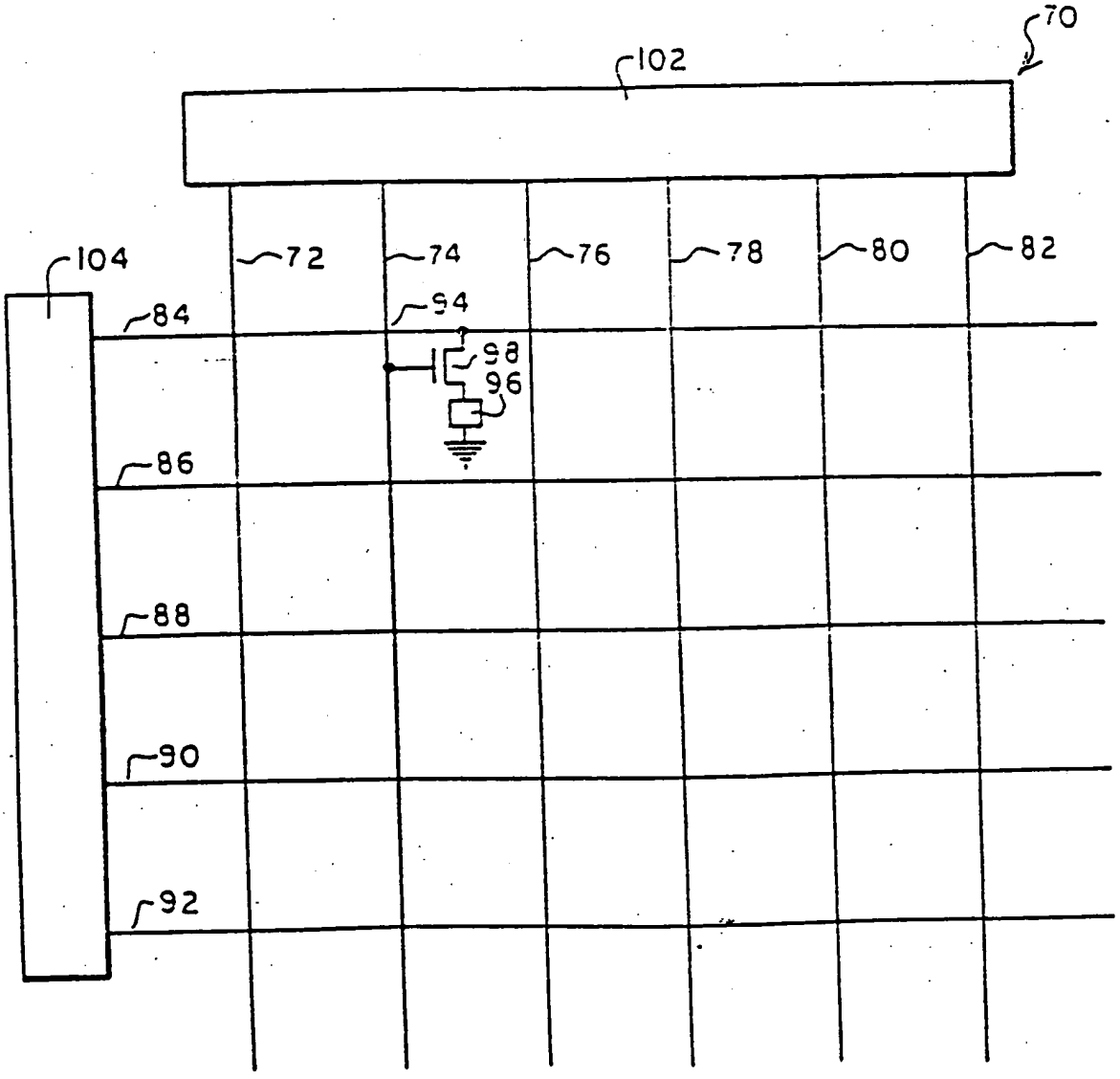
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FIG. 2